CLAIM AMENDMENTS

The claims are amended as follows.

1. (Currently Amended) A method comprising:

extracting parameters of a set of domino logic circuits, each domino logic circuit of the set of domino logic circuits having inputs and an output;

simulating each domino logic circuit of the set of domino logic circuits, each domino logic circuit simulated after any domino logic circuit feeding into at least one of the inputs of the domino logic circuit has been simulated; and

reporting results of the simulating indicating whether any of the domino logic circuits is likely to generate an erroneous output.

2. (Cancelled)

3. (Previously Amended) The method of claim 1 wherein:

simulating each domino logic circuit includes using the simulated results of circuits coupled to the inputs of the domino logic circuit.

4. (Currently Amended) A method, comprising:

scheduling a set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list; ~~and~~

simulating each domino logic circuit according to the ordered list~~.~~; and

determining whether any of the domino logic circuits is likely to generate an erroneous output.

5. (Original) The method of claim 4 further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits.

6. (Original) The method of claim 5 further comprising:

reporting results of the simulating.

7. (Cancelled)

8. (Previously Amended) The method of claim 6 wherein:

the extracting further including extracting parameters of non-domino circuits;

the scheduling further including scheduling non-domino circuits into the ordered list; and

the simulating further including simulating non-domino circuits.

9. (Original) The method of claim 8 wherein:

the reporting further including reporting results of the simulating non-domino circuits.

10. (Currently Amended) A machine readable medium embodying instructions which, when executed by a processor, cause the processor to perform a method, the method comprising:

scheduling a set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list; and

simulating each domino logic circuit according to the ordered list~~.~~; and

determining whether any of the domino logic circuits is likely to generate an erroneous output.

11. (Original) The machine readable medium of claim 10 further embodying instructions which, when executed by a processor, cause the processor to perform the method further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits.

12. (Original) The machine readable medium of claim 11 further embodying instructions which, when executed by a processor, cause the processor to perform the method further comprising:

reporting results of the simulating.

13. (Cancelled)

14. (Previously Amended) The machine readable medium of claim 12 further embodying instructions which, when executed by a processor, cause the processor to perform the method wherein:

the extracting further including extracting parameters of non-domino circuits;

the scheduling further including scheduling non-domino circuits into the ordered list; and

the simulating further including simulating non-domino circuits.

15. (Currently Amended) A system comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller;

wherein the processor executes instructions to perform the method of:

scheduling a set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list; ~~and~~

simulating each domino logic circuit according to the ordered list~~.~~; and

reporting results of the simulating indicating whether any of the domino logic circuits is likely to generate an erroneous output.

16. (Currently Amended) The system of claim 15 wherein the processor further executes instructions to perform the method further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits.~~; and~~

~~reporting results of the simulating.~~

17. (Currently Amended) An apparatus comprising:

means for extracting parameters for each domino logic circuit of a set of domino logic circuits;

means for scheduling the set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list;

means for simulating each domino logic circuit according to the ordered list

means for reporting results of the means for simulating, the results indicating whether any of the domino logic circuits is likely to generate an erroneous output.

18. (Currently Amended) The method of claim 3 wherein:

simulating each domino logic circuit includes ~~generating output results of each domino logic circuit, the output results including~~ determining worst-case noise that will be generated by each domino logic circuit.

19. (Cancelled)

20. (Currently Amended) The method of claim 4 wherein:

simulating each domino logic circuit includes ~~generating output results of each domino logic circuit, the output results including~~ determining worst-case noise that will be generated by each domino logic circuit.

21. (Cancelled)

22. (Currently Amended) The machine readable medium of claim 10, further embodying instructions which, when executed by a processor, cause the processor to perform the method wherein:

simulating each domino logic circuit includes ~~generating output results of each domino logic circuit, the output results including~~determining worst-case noise that will be generated by each domino logic circuit.

23. (Cancelled)

24. (Currently Amended) The system of claim 15 wherein:

simulating each domino logic circuit includes ~~generating output results of each domino logic circuit, the output results including~~determining worst-case noise that will be generated by each domino logic circuit.

25. (Cancelled)

26. (Currently Amended) The system of claim 17 wherein:

means for simulating each domino logic circuit includes ~~generating output results of each domino logic circuit, the output results including~~determining worst-case noise that will be generated by each domino logic circuit.

27. (Cancelled)